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EXAMINER	
ALI, SYED J	
ART UNIT	PAPER NUMBER
2127	10

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	**Application No.** 09/531,397	**Applicant(s)** BALLANTYNE, JOSEPH C.	
	Examin r Syed J Ali	**Art Unit** 2127	

-- The MAILING DATE of this communication appears on the cover she t with th correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *July 23, 2003* .

2a)☒ This action is **FINAL**.   2b)□ This action is non-final.

3)□ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-9,11 and 13-33* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)□ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9,11 and 13-33* is/are rejected.

7)□ Claim(s) _____ is/are objected to.

8)□ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)□ The specification is objected to by the Examiner.

10)□ The drawing(s) filed on _____ is/are: a)□ accepted or b)□ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)□ The proposed drawing correction filed on _____ is: a)□ approved b)□ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)□ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)□ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)□ All b)□ Some * c)□ None of:

1.□ Certified copies of the priority documents have been received.

2.□ Certified copies of the priority documents have been received in Application No. _____ .

3.□ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)□ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) □ The translation of the foreign language provisional application has been received.

15)□ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) □ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) □ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) □ Interview Summary (PTO-413) Paper No(s). _____ .
5) □ Notice of Informal Patent Application (PTO-152)
6) □ Other: .

DETAILED ACTION

1. This office action is in response to Amendment A, paper number 9, which was received July 23, 2003. Applicant's arguments have been fully considered but they deemed to be moot in view of the new ground of rejection. Claims 1-9, 11, and 13-33 are presented for examination.

2. The text of those sections of Title 35, U.S. code not included in this office action can be found in a prior office action.

Claim Rejections - 35 USC § 102

3. Claim 13 is rejected under 35 U.S.C. 102(e) as being anticipated by Gulick (USPN 6,421,702).

As per claim 13, Gulick discloses a method of scheduling resources on at least one microprocessor that includes a CPU and a device, the method comprising the steps of:

a. using the device to determine when to allocate the resources in real-time (col. 5 lines 14-21, "Timer 228 provides a real-time hardware interrupt to CPU 102. At a predefined interval, timer 228 outputs a signal that asserts an interrupt");

b. causing the device to issue a non-maskable interrupt to the CPU when it is time to allocate the resources (col. 11 lines 3-23, "If the task does not complete within the specified maximum duration, termination unit 224 may invoke an interrupt to terminate the task. In one embodiment, the interrupt invoked is a non-maskable interrupt"); and

c. causing the CPU to allocate the resources in response to the non-maskable interrupt (col. 7 lines 4029, "scheduler 218 may determine whether sufficient resources are available to service the tasks based upon the available portion of the operating system cycle for isochronous tasks and the resources used by other isochronous tasks. If sufficient resources are available, scheduler 218 schedules the isochronous tasks of the application").

Claim Rejections - 35 USC § 103

4. Claims 1-7, 9, 11, 14-21, and 23-33 are rejected under 35 U.S.C. 103(a) as being unpatentable over Reiffin (USPN 6,330,583) (hereinafter Reiffin) in view of Gulick.

As per claim 1, Reiffin discloses a method of scheduling CPU resources comprising the steps of:

a. using a counter to determine when to allocate the CPU resources (col. 4 lines 1-14, "When the end of the current timeslice is thereby determined by the counter the latter then signals the interrupt controller which in turn activates the interrupt input of the CPU");

b. instructing an interrupt controller to allocate the CPU resources (col. 4 lines 1-32, "Control of the CPU is then passed to an interrupt service routine which contains or invokes the scheduler for a determination as to the next task to be executed", wherein the interrupt service routine utilizes an interrupt controller to allocate resources associated with a new task to be scheduled).

Gulick discloses the following limitation not shown by Reiffin, specifically:

c. instructing the CPU to allocate resources in real-time (col. 5 lines 14-21, "Timer 228 provides a real-time hardware interrupt to CPU 102. At a predefined interval, timer 228 outputs a signal that asserts an interrupt") by the interrupt controller issuing non-maskable interrupts to the CPU (col. 11 lines 3-23, "If the task does not complete within the specified maximum duration, termination unit 224 may invoke an interrupt to terminate the task. In one embodiment, the interrupt invoked is a non-maskable interrupt").

It would have been obvious to one of ordinary skill in the art to modify Reiffin by adding Gulick to support a wider array of applications. Specifically, Reiffin discloses interrupting a CPU to initiate a context switch when the timeslice of the currently executing application has expired. However, timeslices within Reiffin are static in length, and thus do not support real time applications that may have variable deadlines and performance objectives and priorities. Thus, by combining Reiffin with the disclosure of Gulick of allowing varying durations of timeslices such that real time applications can be supported allows the use of more modern applications that make use of real time. Further, since real time applications have strict deadlines, it is imperative that a provision exists for applications that fail to meet their deadline, such that additional applications do not also miss their deadline due to an earlier overrun. Gulick provides this by issuing a non-maskable interrupt if the task does not complete within its maximum allotted duration. To that end, Gulick provides a method of modifying Reiffin such that a wider variety of applications can be supported that are in accordance with modern computing demands.

As per claim 2, Gulick discloses the method of claim 1 wherein only a portion of the CPU resources are allocated (col. 7 lines 3-29, "the portion of the operating system bandwidth allocated to isochronous tasks may be limited").

As per claim 3, Gulick discloses the method of claim 1 wherein all of the CPU resources are allocated (col. 7 lines 3-29, "a user via user interface 220 may increase the percentage of the operating system bandwidth allocated to isochronous tasks", wherein the percentage could conceivably be adjusted such that the entirety of the operating resources are allocated to isochronous tasks).

As per claim 4, Gulick discloses the method of claim 2 wherein the CPU resources are allocated to at least one thread, and the CPU resources are allocated by determining a duration of time (col. 6 lines 8-17, "Scheduler 218 may additionally output a signal to termination module 224 indicating the duration of an isochronous task") and a periodicity for execution of said at least one thread (col. 5 lines 14-21, "the period of the time-slice interrupt is variable based on the interval of the currently executing isochronous tasks").

As per claim 5, Gulick discloses the method of claim 3 wherein the CPU resources are allocated to at least one thread, and the CPU resources are allocated by determining a duration of time (col. 6 lines 8-17, "Scheduler 218 may additionally output a signal to termination module 224 indicating the duration of an isochronous task") and a periodicity for execution of said at least one thread (col. 5 lines 14-21, "the period of the time-slice interrupt is variable based on the interval of the currently executing isochronous tasks").

As per claim 6, Reiffin discloses the method of claim 1 wherein the counter is a performance counter (col. 4 lines 1-13, "A counter tallies the clock ticks", wherein Applicant states on pg. 13 "that the performance counter 200 could be any type of programmable or re-settable counter", including counting a clock cycle).

As per claim 7, Reiffin discloses the method of claim 6 wherein the performance counter counts machine cycles in order to determine when to allocate the CPU resources (col. 4 lines 1-13, "A counter tallies the clock ticks", wherein each clock tick corresponds to a machine cycle).

As per claim 9, Reiffin discloses the method of claim 1 wherein the counter issues a first interrupt to the interrupt controller in order to instruct the interrupt controller to allocate the CPU resources (col. 4 lines 1-13, "the counter...then signals the interrupt controller which in turn activates the interrupt input of the CPU (central processing unit) to initiate an interrupt operation").

As per claim 11, Gulick discloses the method of claim 9 wherein the first interrupt is non-maskable (col. 11 lines 3-23, "If the task does not complete within the specified maximum duration, termination unit 224 may invoke an interrupt to terminate the task. In one embodiment, the interrupt invoked is a non-maskable interrupt").

As per claim 14, Reiffin discloses the method of claim 13 wherein the device is a performance counter (col. 4 lines 1-13, "A counter tallies the clock ticks", wherein Applicant states on pg. 13 "that the performance counter 200 could be any type of programmable or re-settable counter", including counting a clock cycle). The motivation for combining Reiffin and Gulick is provided above in reference to claim 1.

As per claim 15, Reiffin discloses the method of claim 13 wherein the device is a timer (col. 4 line 1-13, "A clock periodically emits timing pulses or ticks at a high frequency", wherein the clock is analogous to a timer).

As per claim 16, Reiffin discloses a method of scheduling resources on at least one microprocessor that include at least one performance counter, at least one programmable interrupt controller and at least one CPU, said method comprising the steps of:

a. allowing the CPU to execute a first thread (col. 4 lines 1-13, wherein circumstances are described where an interrupt may be serviced, and thus the CPU would be executing a first task at the time of interruption);

b. using the performance counter to determine when to allocate the resources to a second thread (col. 4 lines 1-13, "the counter...then signals the interrupt controller which in turn activates the interrupt input of the CPU", wherein when the interrupt controller activates the interrupt input of the CPU thereby relinquishing control from the first task to the second task);

c. issuing a first interrupt from the performance counter to the programmable interrupt controller when it is time to allocate the resource to the second thread (col. 4 lines 1-13, “the counter...then signals the interrupt controller”);

d. instructing the programmable interrupt controller to issue a second non-maskable interrupt to the CPU that instructs the CPU to switch execution from the first thread to the second thread (col. 4 lines 1-32, “the counter...then signals the interrupt controller which in turn activates the interrupt input of the CPU”, “control of the CPU is taken away from the executing task which is thereby asynchronously preempted”);

e. instructing the CPU to stop execution of the first thread (col. 4 lines 14-32, “control of the CPU is taken away from the executing task which is thereby asynchronously preempted”);

f. causing the CPU to store first current state information regarding execution of the first thread (“Official Notice” is taken that it is well known and expected in the art to store state information of a preempted thread in a multithreaded environment, and since Reiffin states that the executing task is preempted, it follows that it would have been obvious to store state information);

g. causing the CPU to restore second current state information regarding execution of the second thread (“Official Notice” is taken that it is well known and expected in the art to restore state information of a previously suspended or blocked thread, and since Reiffin discusses multithreading, it follows that it would have been obvious to restore state information regarding the thread assuming control of the CPU); and

h. allocating resources to the second thread (col. 4 lines 33-40, "The scheduler signals its task selection to the CPU which then normally executes either the scheduled local task or the scheduled network task", wherein once the next task to be scheduled is selected, CPU resources are allocated to that thread).

Gulick discloses the following limitations not shown by Reiffin, specifically that the interrupts are non-maskable interrupts (col. 11 lines 3-23, "If the task does not complete within the specified maximum duration, termination unit 224 may invoke an interrupt to terminate the task. In one embodiment, the interrupt invoked is a non-maskable interrupt"), and that resources are allocated on a real-time basis (col. 5 lines 14-21, "Timer 228 provides a real-time hardware interrupt to CPU 102. At a predefined interval, timer 228 outputs a signal that asserts an interrupt"). The motivation for combining Reiffin and Gulick is provided above in reference to claim 1.

As per claim 17, Reiffin discloses the method of claim 16 wherein the programmable interrupt controller is an APIC. The discussion of claim 16 discusses the programmable interrupt controller, and an APIC is defined to be a programmable interrupt controller that can handle interrupts from and for multiple CPUs. Therefore, since Reiffin discloses that is for use in a multiprocessor system (Abstract, "The computer time and processing power which would otherwise be wasted while waiting for slow input/output operation is instead utilized to provide a powerful parallel multiprocessor system for handling compute-intensive tasks too large for an individual workstations"), Reiffin inherently discloses that the programmable interrupt controller is an APIC.

As per claim 18, Gulick discloses the method of claim 17 wherein the microprocessor is selected from the group consisting of: a Pentium 4GB, a Pentium Pro 64GB, a Pentium MMX 4GB MMX, a Pentium II 4GB MMX, a Pentium II 4GB MMX KNI, a Celeron 4GB MMX, a Xeon PII 64GB MMX and a Xeon PIII 64GB MMX KNI (col. 4 lines 19-32, "The chipset 106 includes arbitration logic 107 as shown. In one embodiment, the chipset is the Triton chipset available from Intel Corporation", wherein the disclosure is easily modifiable to include any of a number of chipsets, and as the claimed microprocessors are all of the Intel family of processors, the disclosure of Gulick therein satisfies this limitation).

As per claim 19, Reiffin discloses a computer-readable medium having computer-executable instructions stored for performing steps comprising:

a. using a scheduler to control execution of at least one thread (col. 4 lines 1-32, "Control of the CPU is then passed to an interrupt service routine which contains or invokes the scheduler for a determination as to the next task to be executed");

b. using at least one counter to notify the scheduler when to switch execution of said at least one thread (col. 4 lines 1-14, "When the end of the current timeslice is thereby determined by the counter the latter then signals the interrupt controller which in turn activates the interrupt input of the CPU").

Gulick discloses the following limitation not shown by Reiffin, specifically that the scheduling of tasks in done on a real-time basis (col. 5 lines 14-21, "Timer 228 provides a real-time hardware interrupt to CPU 102. At a predefined interval, timer 228 outputs a signal that asserts an interrupt"). The motivation for combining Reiffin and Gulick is provided above in reference to claim 1.

As per claim 20, Reiffin discloses the computer-readable medium of claim 19 further comprising instructions for issuing an interrupt from the counter when the counter reaches a predetermined number (col. 4 lines 1-13, "A counter tallies the clock ticks until the total reaches a predetermined number"), said predetermined number defining a maximum duration for execution of said at least one thread (col. 4 lines 1-13, "a predetermined number which determines the time duration of each timeslice"), said interrupt notifying the scheduler to switch execution to another thread (col. 4 lines 1-13, "the counter…then signals the interrupt controller which in turn activates the interrupt input of the CPU…to initiate an interrupt operation").

As per claim 21, Reiffin discloses the computer-readable medium of claim 20 wherein said at last one counter is a performance counter and counts CPU cycles (col. 4 lines 1-13, "A counter tallies the clock ticks", wherein the clock ticks correspond to CPU cycles).

As per claim 23, Reiffin does not specifically disclose the computer-readable medium of claim 20 further comprising instructions for executing said at least one thread at a highest IRQ level. However, "Official Notice" is taken that it would have been obvious to one of ordinary skill in the art to place the interrupting thread at a highest IRQ level since that would ensure that the interrupting task is serviced without being preempted by another task. To that end, threads of a highest priority may be guaranteed Quality of Service, such that tasks of a highest priority are serviced accordingly.

As per claim 24, Reiffin discloses the computer-readable medium of claim 20 further comprising instructions for executing said at least one thread in a transparent manner so that at least one operating-system process is unaware of the execution of said at least one thread (col. 4 lines 41-59, "control of the CPU is rapidly switched back and forth between a local task and a network task so rapidly that the two tasks are said to be running concurrently", wherein the local task could be considered the operating system thread and can be treated simply as a permanent process, and does not need to be made aware of other background processes).

As per claim 25, Gulick discloses the computer-readable medium of claim 24 further comprising instructions for executing all of said operating-system process and all of said at least one threads as a single real-time thread (col. 1 line 48 - col. 2 line 35, "Several partially effective methods of providing real-time capability to general-purpose operating systems have been used", wherein Gulick discloses how a real-time interrupt can be used within a general purpose operating system to execute all processes therein as a single real-time process).

As per claim 26, Gulick discloses the computer-readable medium of claim 20 wherein the duration for execution of said at least one thread is not equal to the duration for execution of said another thread (col. 7 lines 29-46, "Each task lists its interval and execution duration. The interval, or rate, specifies how often the isochronous task should be executed and the execution duration identifies the specified maximum execution time")

As per claim 27, Gulick discloses the computer-readable medium of claim 19 further comprising instructions for allocating at least a portion of a CPU's resources to an operating-system process and using the remaining CPU resources for execution of said at least one thread (col. 7 lines 4029, "scheduler 218 may determine whether sufficient resources are available to service the tasks based upon the available portion of the operating system cycle for isochronous tasks and the resources used by other isochronous tasks. If sufficient resources are available, scheduler 218 schedules the isochronous tasks of the application", wherein the CPU resources are divided among the operating system bandwidth and the isochronous tasks to be executed).

As per claim 28, Gulick discloses the computer-readable medium of claim 27 further comprising instructions for releasing the CPU resources back to the operating-system process when said at least one thread finishes execution (col. 7 lines 18-29, "a user via user interface 220 may increase the percentage of the operating system bandwidth allocated to isochronous tasks", wherein once the task has been completed, the user may then reallocate the operating system bandwidth to give CPU resources back to the operating system).

As per claim 29, Reiffin discloses the computer-readable medium of claim 27 further comprising instructions for releasing the CPU resources to another thread when said at least one thread finished execution (col. 4 lines 33-40, "At the start of the next timeslice the counter is reset and the above-described cycle of operation is iterated over and over again", wherein the cycle of servicing tasks through the use of interrupts is disclosed, and upon completion of a timeslice, the yielding thread returns the CPU resources to the system).

As per claim 30, Gulick discloses the computer-readable medium of claim 19 further comprising instructions for allocating a predetermined number of CPU cycles for execution of an operating-system process and using the remaining CPU cycles for execution of said at least one thread (col. 7 lines 4029, "scheduler 218 may determine whether sufficient resources are available to service the tasks based upon the available portion of the operating system cycle for isochronous tasks and the resources used by other isochronous tasks. If sufficient resources are available, scheduler 218 schedules the isochronous tasks of the application", wherein the CPU resources are divided among the operating system bandwidth and the isochronous tasks to be executed).

As per claim 31, Applicant discloses Prior Art that states that interrupts can switched from non-maskable to maskable by executing the STI instruction. Thus, the Prior Art already suggests the act of changing an interrupt from non-maskable to maskable.

As per claim 32, Applicant discloses Prior Art that states that interrupts can switched from maskable to non-maskable by executing the CLI instruction. Thus, the Prior Art already suggests the act of changing an interrupt from maskable to non-maskable.

As per claim 33, Reiffin discloses the computer-readable medium of claim 20 wherein said at least one thread and said another thread are of the same priority (col. 4 lines 33-40, wherein the scheduler chooses between a local task and a network task and the decision is made based purely on what the preempted task was. In that sense, the priorities of both tasks are equal since the type of task that was not running in ensured service when the other type of task is preempted).

5. Claims 8 and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Reiffin in view of Gulick in view of Patterson et al. (USPN 6,320,882) (hereinafter Patterson).

As per claim 8, Patterson discloses the following limitations not shown by the modified Reiffin, specifically the method of claim 6 wherein the performance counter counts executed computer instructions (col. 2 line 66 - 3 line 43, "an integer field, functioning as a global counter, is incremented based on a regularly occurring event", "Global counter 222 is incremented based on the output of clock 204, and may be, for example, incremented one 'tick' for every million cycles of clock 204" wherein this is merely one way in which the counter may be set up, and to align the clock such that a tick corresponds to the number of clock cycles necessary for a single instruction to issue is merely another embodiment of the same concept).

It would have been obvious to one of ordinary skill in the art to combine the modified Reiffin with Patterson since within the framework of a real time application environment, restricting the interrupt controller to be triggered by only certain events prevents the environment from being modified to suit particular needs. For example, a real time task may be required to perform a certain amount of work before it is preempted, in addition to having a deadline. To that end, by preempting the task at the expiration of the period, rather than allowing the task to complete a minimum amount of work may cause performance of later tasks to suffer. Allowing the counter to be incremented based on any type of regularly occurring event, such as a computer instruction, allows the capabilities of the system to be modified to suit any number of specific needs.

As per claim 22, Patterson discloses the following limitation not shown by Reiffin, specifically the computer-readable medium of claim 20 wherein said at least one counter is a part of a CPU and counts executed instructions (col. 3 lines 41-43, "Global counter 222 is incremented based on the output of clock 204, and may be, for example, incremented one 'tick' for every million cycles of clock 204" wherein this is merely one way in which the counter may be set up, and to align the clock such that a tick corresponds to the number of clock cycles necessary for a single instruction to issue is merely another embodiment of the same concept displayed by Patterson). The motivation for combining Patterson with Reiffin can be found above in reference to claim 8.

Response to Arguments

6. Applicant argues on page 9 that claims 31 and 32 are not duplicates, as previously objected to in that, "*In claim 31 the interrupt is switched from 'non-maskable to maskable' and in claim 32 the interrupt is switched from 'maskable to non-maskable'*". It is agreed that

although these claims are similar, they are not duplicates, and therefore the objection is withdrawn.

7. Applicant has amended independent claims 1, 13, 16, and 19 to include limitations related to features of the disclosure that support real-time capabilities. Since real-time capabilities were not expressly claimed previously, this necessitated a new search, resulting in the above cited Gulick reference. Since the amendment therein altered the scope of the independent claims, as well as all of the dependent claims therein, new grounds of rejection were necessary to show how the Prior Art disclosed these limitations. All rejections in the previous Office Action are withdrawn, and the above discussion of all the pending claims is considered sufficient in showing how the Prior Art discloses scheduling tasks in real-time using both maskable and non-maskable interrupts.

8. Applicant argues on page 8, "*Reiffin does not teach or suggest 'instructing the CPU to allocate resources in real-time,* '" and also argues on page 12 that "*Bonola also does not disclose this feature.*" As discussed above, Gulick discloses the real-time capabilities that are presently claimed. Therefore, the argument that neither Reiffin nor Bonola disclose the feature of allocating resources in real-time is moot in view of the new grounds of rejection. Further, since the previous rejections have been withdrawn, the argument that "*the Action has failed to provide proper motivation for combining the teachings of Reiffin and Bonola*" is also moot.

9. Applicant contends that the remainder of the claims are allowable for either reciting similar features related to real-time capabilities as in claim 1, or for depending from alleged allowable claims. In accordance with the thorough discussion of all the pending claims that has been presented, it is determined that the present claims are not allowable over the Prior Art.

Conclusion

10. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Syed J Ali whose telephone number is (703) 305-8106. The examiner can normally be reached on Mon-Fri 8-5:30, 2nd Friday off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, William A Grant can be reached on (703) 308-1108. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3900.

Syed Ali
September 17, 2003

MAJID A. BANANKHAH
PRIMARY EXAMINER